UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,919,769 B2
APPLICATION NO. : 10/670828
DATED : July 19, 2005
INVENTOR(S) : Lim et al.

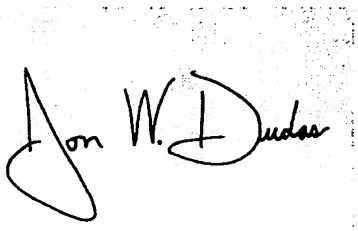
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Drawings:
Fig. 1, "VBP/12" should read -- VBP/124--;
Fig. 6, "INPUT/OUTPUT DEVICE 614" should read --INPUT/OUTPUT MODULE 614--;

In the Claims:
Col. 1, line 52, "VCO 212." should read --VCO 126.--;
Col. 3, line 14, "... voltage of the VCO 212." should read --... voltage of the VCO 126.--;
Col. 4, line 52, "...of flip-flops 252a-252h are..." should read --...of flip-flops 452a-452h are... --;
Col. 5, line 22, "...of the VCO 212..." should read --...of the VCO 126...--;
Col. 5, line 55, "...input/output modules 614 include..." should read --...input/output module 614 include...--;
Col. 6, line 32, "...first flip flop is ..." should read --...first flip-flop is...--;
Col. 6, line 33, "...from an output terminal of a last flip flop." should read --... from an output terminal of a last flip-flop. --;
Col. 6, line 36, "...plurality of flip flops and..." should read --... plurality of flip-flops and...--;
Col. 6, line 37, "...plurality of flip flops." should read --... plurality of flip-flops.--;
Col. 6, line 38, "...last flip flop and..." should read --... last flip-flop and...--;
Col. 7, line 14, "...the central processor unit and..." should read --...the central processing unit ...--;
Col. 7, line 15, "...the central processor unit and the main memory." should read --... the central processing unit and the main memory.--;
Col. 8, line 1, "...first flip flop is..." should read --...first flip-flop is...--;
Col. 8, line 2, "...last flip flop." should read --...last flip-flop.--;

Signed and Sealed this

Twentieth Day of March, 2007



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Director of the United States Patent and Trademark Office